Parallel Integrated Circuit Test Apparatus and Test Method

ABSTRACT

A test apparatus (400) comprising a single handler (404) is coupled to a first tester (436) and second tester (408), wherein the first (436) and second (408) testers are coupled together. A first test procedure is performed on a set of second IC's using the first tester (436), simultaneously while a second test procedure is performed on a first set of IC's using the second tester (408). Sets of IC's may be tested in parallel by a plurality of testers (436/408) within a single handler (404). The first (436) and second (408) testers may be coupled to a multiplexer (460) to allow the use of a single test head (478), which avoids having to make contact to the integrated circuit more than once, which is particularly advantageous in wafer probe testing.